Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.133”**

**ANODE**

**.117 x .117”**

**.133”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .117” X .117”**

**Backside Potential: Cathode**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .133” X .133” DATE: 11/10/21**

**MFG: MICROSEMI / PPC THICKNESS .010” P/N: 1N5814**

**DG 10.1.2**

#### Rev B, 7/19/02